

Abstract of the Disclosure

A memory device verify system determines a state of memory cells in a memory. The memory includes a memory array having a plurality of memory cells coupled to bit lines. A verify circuit is coupled to the bit lines to determine if memory cells have an erase level that is within predetermined upper and lower limits. The verify circuit can include first and second comparators. In one embodiment, the first comparator is used to compare a bit line current with an upper first reference current. The second comparator is used to compare a bit line current with a lower second reference current. The comparator circuit is not limited to reference currents, but can use reference voltages to compare to a bit line voltage. The verify circuit, therefore, eliminates the need for separate bit line leakage testing to identify over-erased memory cells. Memory verify methods using two reference signal are also provided.

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